

Nanodevices by using semiconductor nanowires

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ABSTRACT

One-dimensional semiconductor nanowires have attracted increasing interest due to their novel physical properties and diversity for potential electronic and photonic device applications. The Vapor-Liquid-Solid (VLS) mechanism for nanowires growth is explained in Experiment section. Recent studies have demonstrated that semiconductor nanowires would be attractive building blocks for assembling electronic and optoelectronic nanosystems. A number of nanodevices, such as FETs,⁷ bipolar transistors,⁸ inverters,⁹ light emitting diodes (LED),¹⁰ and even logic gates,¹¹ have been assembled from well-defined semiconductor nanowires. P-n junction result of Si nanowires is shown as a simple example of nanowire building blocks. Another big step toward nanodevices was achieved by core-multishell structures of semiconductor nanowires. Those Core-multishell structures, including a high performance coaxially gated field-effect transistor, shows the general potential of radial heterostructure growth for the development of nanowire-based devices.

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INTRODUCTION

One-dimensional nanostructures such as nanowires (NWs) and nanotubes are attractive building blocks for nanoelectronics since their morphology, size, and electronic properties make them suitable for fabricating both nanoscale devices and interconnects.¹ For example, single-walled carbon nanotubes have been used as building blocks to fabricate room temperature field effect transistors (FETs),² diodes,³ and recently an inverter.⁴ However, there are substantial limitations on the use of nanotubes for integrated nanoelectronics or even simple device arrays, because semiconducting and metallic nanotubes are obtained simultaneously during growth.^{1,5} In contrast, recent studies have demonstrated that the chemical and physical characteristics of NWs, including composition, size, electronic and optical properties, can be rationally controlled during synthesis in a predictable manner,⁶ thus making these materials attractive building blocks for assembling electronic and optoelectronic nanosystems. For an example, a number of nanodevices, such as FETs,⁷ bipolar transistors,⁸ inverters,⁹ light emitting diodes (LED),¹⁰ and even logic gates,¹¹ have been assembled from these well-defined semiconductor NWs. Core-multishell structures, including a high performance coaxially gated field-effect transistor, shows the general potential of radial heterostructure growth for the development of nanowire-based devices.

Experiment I: Vapor-Liquid-Solid Nanowire Growth

Recently, semiconductor nanowires with different compositions have been successfully synthesized using either vapor⁹ or solution-based methodologies.¹¹ One key feature of these syntheses is the promotion of anisotropic crystal growth using metal nanoparticles as catalysts.

The growth mechanism has been extrapolated from the vapor-liquid-solid (VLS) mechanism which was proposed in the 1960s-1970s for large whisker growth.¹²

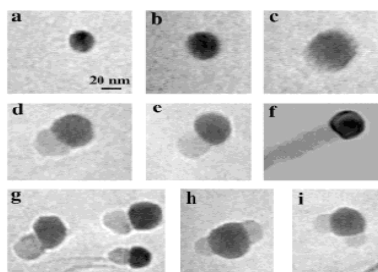


Figure 1. In situ TEM images recorded during the process of nanowire growth. (a) Au nanoclusters in solid state at 500 °C; (b) alloying initiates at 800 °C, at this stage Au exists in mostly solid state; (c) liquid Au/Ge alloy; (d) the nucleation of Ge nanocrystal on the alloy surface; (e) Ge nanocrystal elongates with further Ge condensation and eventually a wire forms (f). (g) Several other examples of Ge nanowire nucleation. (h,i) TEM images showing two nucleation events on single alloy droplet.

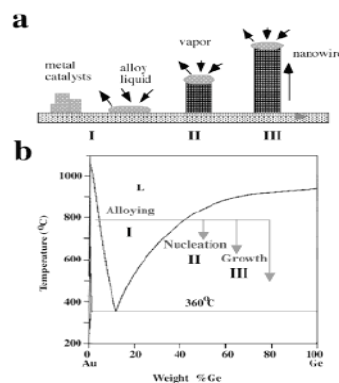


Figure 2. (a) Schematic illustration of vapor-liquid-solid nanowire growth mechanism including three stages (I) alloying, (II) nucleation, and (III) axial growth. The three stages are projected onto the conventional Au-Ge binary phase diagram (b) to show the compositional and phase evolution during the nanowire growth process.

Peidong Yang's group have published a good example to understand this VLS mechanism a few years ago.¹⁴ Figure 1a-f shows a sequence of TEM images during the growth of a Ge nanowire in situ. This real-time observation of the nanowire growth directly mirrors the VLS mechanism in Figure 2a. They have examined over 50 individual Au clusters during the in situ catalytic nanowire growth. In general, three stages (I-III) could be clearly identified.

(I): *Alloying process (Figure 1a-c)*. Au clusters remain in the solid state up to their maximum experimental temperature 900°C if there is no Ge vapor condensation. With increasing amount of Ge vapor condensation and dissolution, Ge and Au form an alloy and liquefy. The volume of the alloy droplets increases, and the elemental contrast decreases (due to dilution of the heavy metal Au with the lighter element Ge) while the alloy composition crosses sequentially,^{??} from left to right, a biphasic region (solid Au and Au/Ge liquid alloy) and a single phase region

(liquid). This alloying process can be depicted as an isothermal line in the Au-Ge phase diagram (Figure 2b).

(II): *Nucleation (Figure 1d,e)*. Once the composition of the alloy crosses the second liquidus line, it enters another biphasic region (Au/Ge alloy and Ge crystal). This is where nanowire nucleation starts. Knowing the alloy volume change, they estimate that the nucleation generally occurs at Ge weight percentage of 50-60%. This value differs from the composition calculated from the equilibrium phase diagram which indicates the first precipitation of Ge crystal should occur at 40% Ge (weight) and 800 °C. This difference indicates that the nucleation indeed occurs in a supersaturated alloy liquid. Interestingly, they have also occasionally observed that two Ge nanocrystals precipitate from single alloy droplets and create two liquid/solid interfaces (Figure 1h,i).¹⁵ The finite volume of the alloy liquid, on the order of 10^{-17} cm^{-3} , apparently limits the number of possible heterogeneous nucleation events,¹⁶ unlike those microscopic systems where tens or hundreds of whiskers can be observed on single alloy droplet.¹²

(III). *Axial growth (Figure 1d-f)*. Once the Ge nanocrystals nucleate at the liquid/solid interface, further condensation/dissolution of Ge vapor into the system will increase the amount of Ge crystal precipitation from the alloy. This can be readily accounted for, using the famous lever rule of phase diagram. The incoming Ge species prefer to diffuse to and condense at the existing solid/liquid interface, primarily due to the fact that less energy will be involved with the crystal step growth as compared with secondary nucleation events in a finite volume. Consequently, secondary nucleation events are efficiently suppressed, and no new solid/liquid interface will be created. The existing interface will then be pushed forward (or backward) to form a nanowire (Figures 1f, 2b). After the system cools, the alloy droplets solidify on the nanowire tips.

Experiment II: How to position nanowires where they are wanted

After we grow semiconductor nanowires, the next step would be how we can position those nanowires where they are wanted. Because a nanowire is elongated, and so easily electrically polarized, it is attracted towards a high electric field, with which it lines up. So when a voltage is applied between two electrodes, a nearby nanowire suspended in liquid is drawn in to bridge the gap between them (Fig. 2). Recent work has produced orderly rows of parallel single-nanowire bridges in this way.^{??} Duan *et al.*^{??} have now created a junction by placing a p-doped and an n-doped nanowire across each other.

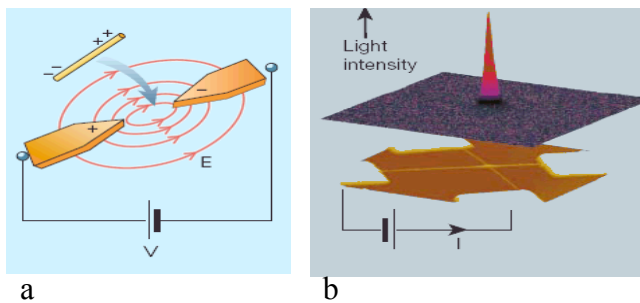


Figure 2. **a**, The nanowire is assembled between two metal electrodes using an electric field gradient. **b**, In the experiment of Duan *et al.*, a p-doped and n-doped nanowire are crossed to form a nanoscale light-emitting diode.

RECENT RESULTS

The first development of nanodevices by using semiconductor nanowires was achieved by Charles Lieber's group. In their paper (*Science* **291**, 851), boron- and phosphorous doped silicon nanowires were used as building blocks to assemble three types of semiconductor nanodevices. Crossed Si nanowire junction is shown in fig.3. Field emission scanning electron microscopy (FESEM) was used to image a typical *p-n* junction assembled from 20-nm-diameter *p*- and *n*-type Si nanowires (Fig. 3A). Current versus voltage (*I-V*) data recorded on the

individual p - and n -type Si nanowires (Fig. 3B) are linear and indicate that metal-Si nanowire contacts are ohmic, and thus will not make a significant contribution to the I - V behavior of the junctions. Significantly, four-terminal I - V measurements made on the p - n junction formed at the nanowire-nanowire cross show good current rectification (Fig. 3B). These nanoscale junctions thus exhibit similar behavior to bulk semiconductor p - n junctions. They also have developed logic gates and computation from assembled nanowire building blocks.¹⁹ In their works, they showed the first step toward a “bottom-up” fabrication technique for electronics manufacturing.

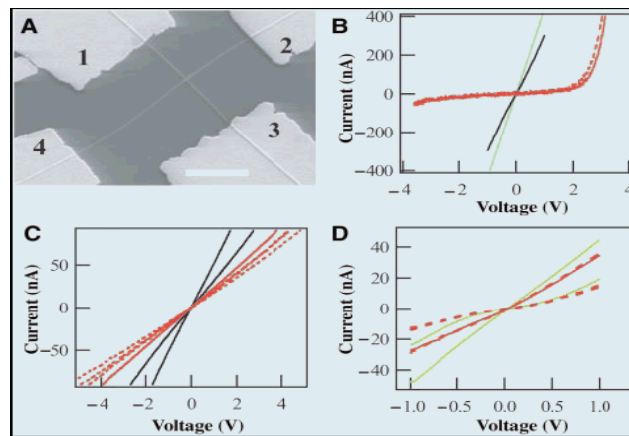


Figure 3. (A) Typical FESEM image of a crossed Si nanowire junction with Al/Au contacts. The scale bar is 2 μ m. The diameters of the nanowires used in these studies ranged from 20 to 50 nm. (B through D) I - V behavior of p - n , p - p , and n - n junctions, respectively. The black and green curves correspond to the I - V behavior of individual p - and n -type Si nanowires, respectively. The red curves represent I - V behavior of junctions. (B) The red curves correspond to four-terminal I - V through the p - n junction; the current values are multiplied by 10. The solid line corresponds to voltage drop measured between leads 3 and 4, and the dashed line to voltage between 3 and 2. (C and D) The red curves are two-terminal I - V through p - p and n - n junctions, respectively. The solid lines correspond to data from contacts 1-2, and the dashed lines correspond to data from the other three pairs (that is, 1 and 4, 2 and 3, and 3 and 4).

Lieber’s group has made another big step toward nanodevices in their next nature paper.²⁰

They suggested that core–shell heterostructures formed by the growth of crystalline overlayers

on nanocrystals offer enhanced emission efficiency²¹, important for various applications.²² Then, they synthesize silicon and germanium core–shell and multishell nanowire heterostructures using a chemical vapour deposition method applicable to a variety of nanoscale materials. (Fig. 4)

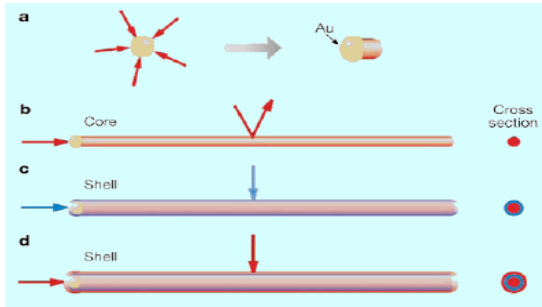


Figure 4 Synthesis of core–shell nanowires by chemical vapour deposition. **a**, Gaseous reactants (red) catalytically decompose on the surface of a gold nanocluster leading to nucleation and directed nanowire growth. **b**, One-dimensional growth is maintained as reactant decomposition on the gold catalyst is strongly preferred. **c**, Synthetic conditions are altered to induce homogeneous reactant decomposition on the nanowire surface, leading to a thin, uniform shell (blue). **d**, Multiple shells are grown by repeated modulation of reactants.

Based on this core-multishell nanowire heterostructure approach, they have prepared new device structures, such as a coaxially gated nanowire field-effect transistor (FET) (Fig. 5). The coaxial geometry offers advantages for nano-FETs, such as a capacitance enhancements compared to standard planar gates used in nanowire²³ and nanotube²⁴ FETs, and might be best compared to double-gated structures being investigated for advanced planar devices.²⁵ The nanowire building blocks used to fabricate coaxial FETs consisted of a core–multishell structure: p-Si/i-Ge/SiO_x/p-Ge, where the active channel is the i-Ge shell.

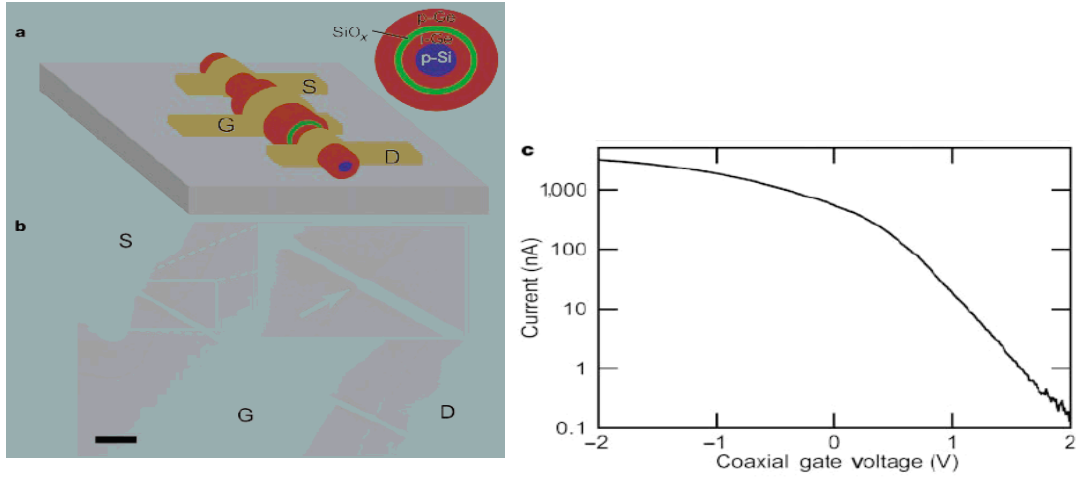


Figure 5 Coaxially-gated nanowire transistors. **a**, Device schematic showing transistor structure. The inset shows the cross-section of the as-grown nanowire, starting with a p-doped Si core (blue, 10 nm) with subsequent layers of i-Ge (red, 10 nm), SiO_x (green, 4 nm), and p-Ge (5 nm). The source (S) and drain (D) electrodes are contacted to the inner i-Ge core, while the gate electrode (G) is in contact with the outer p-Ge shell and electrically isolated from the core by the SiO_x layer. **b**, Scanning electron micrograph (SEM) of a coaxial transistor. Source and drain electrodes were deposited after etching the Ge (30% H₂O₂, 20 s) and SiO_x layers (buffered HF, 10 s) to expose the core layers. The etching of these outer layers is shown clearly in the inset and is indicated by the arrow. The gate electrodes were defined in a second step without any etching before contact deposition. Scale bar is 500 nm. **c**, Gate response of the coaxial transistor at V_{SD} = 1 V, showing a maximum transconductance of 1,500 nA V⁻¹. Charge transfer from the p-Si core to the i-Ge shell produces a highly conductive and gateable channel.

It is also interesting that they have produced field-effect transistors based on the metal/semiconductor nanowire heterostructures by applying their technique of core-multishell nanowire growth.²⁶ The atomically sharp metal–semiconductor interfaces produced in these

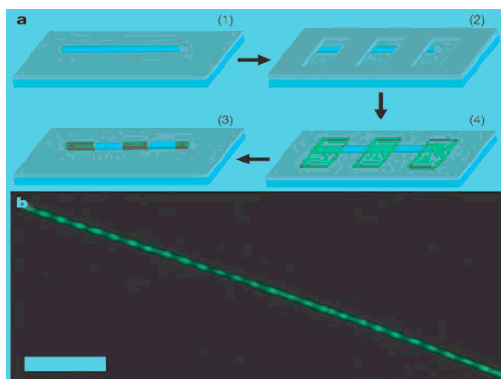


Figure 6 a, Fabrication of NiSi/Si nanowire heterostructures and superlattices. (1) Si nanowires (blue) dispersed on a substrate are (2) coated with photoresist (grey) and lithographically patterned, (3) selectively coated with Ni metal (green) to a total thickness comparable to the Si nanowire diameter, and (4) reacted at 550 °C to form NiSi nanowires. **b**, Dark-field optical image of a single NiSi/Si nanowire heterostructure. The bright green

nanowire heterostructures have the potential to yield a range of precisely defined electronic devices and device arrays on individual nanowires. To explore this opportunity they have prepared field-effect transistor (FET) devices in which the critical source–drain regions are defined by metallic NiSi nanowire sections on p-type Si nanowire. Current versus source–drain voltage (V_{sd}) data (Fig. 7) are linear to $|V_{sd}| \leq 1$ V, which suggests that the NiSi/Si contacts behave for practical purposes as ohmic contacts at room temperature, although preliminary temperature-dependent measurements show a barrier at low temperature. The room temperature behavior can be explained by the reported segregation of dopant to the NiSi/Si interface during NiSi formation²⁷, although other factors may also contribute to the ohmic response at room

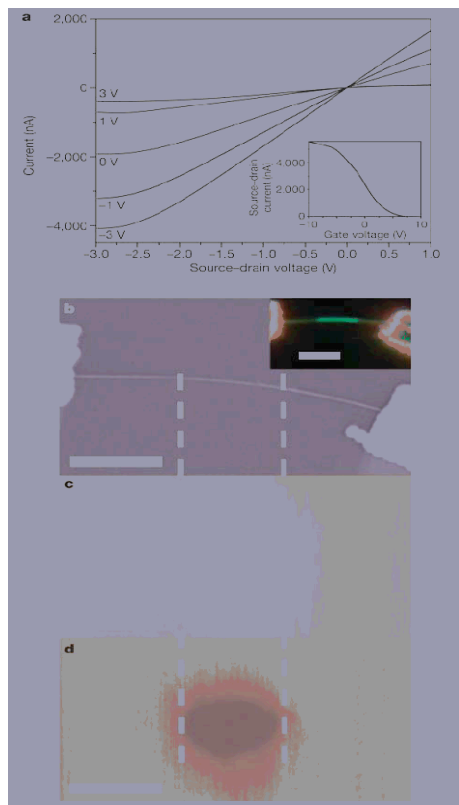


Figure 7 Transport properties of a NiSi/p-Si/NiSi heterojunction field-effect transistor. **a**, I versus V_{sd} , exhibiting the typical characteristics of a NiSi/p-Si/NiSi heterojunction transistor. Inset, gate sweep obtained from the same device in the saturation regime with $V_{sd} = -3$ V. The device was fabricated using a 30-nm diameter p-Si nanowire (dopant density = $\sim 1 \times 10^{18} \text{ cm}^{-3}$) on a heavily doped silicon substrate with 600 nm of thermal oxide; the channel length is 3 μm . **b**, SEM image of a field-effect transistor device fabricated using a NiSi/p-Si/NiSi nanowire heterojunction. Inset, dark-field optical image of the same device, where the bright green segment corresponds to silicon and the dark segments to NiSi. Scale bars, 3 μm . **c and d**, SGM images show reduced conductance with +9 V (Fig. 4c) and enhanced conductance with -9 V gate voltage (Fig. 7d) on the atomic force microscope tip. The dotted lines mark the interface between the NiSi and p-Si regions. Scale bars, 3 μm .

temperature. Notably, $I-V_{sd}$ data recorded at different back gate voltages (V_g) exhibit the behavior expected²⁸ of a depletion mode p-FET with a high hole mobility of $325 \text{ cm}^2 \text{ V}_s^{-1}$.

SUMMARY

Substantial effort has been placed on developing semiconducting nanowires as building blocks for electronic devices – such as field effect transistors – that could replace conventional silicon transistors in hybrid electronics or lead to stand-alone nanosystems. Lieber's group has shown the most impressive results in this challenging field up to now. Recent their studies have demonstrated that semiconductor nanowires would be attractive building blocks for assembling electronic and optoelectronic nanosystems. Even logic gates were developed from well-defined semiconductor nanowires. Furthermore, another big step toward nanodevices was achieved by core-multishell structures. Those Core-multishell structures, including a high performance coaxially gated field-effect transistor, shows the general potential of radial heterostructure growth for the development of nanowire-based devices.

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